# MULTI-CHIP RECEIVE MODULE FOR A WIDE-BAND X-BAND DUAL-BEAM PHASED ARRAY COMMUNICATION ANTENNA

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## ABSTRACT

A wide-bandwidth X-band receive module has been developed to support a phased array communication antenna with dual-beam operation. The module utilizes four GaAs MMIC's, a single low-temperature-cofired-ceramic (LTCC) substrate, blind-mate connectors, and a custom miniature DC/control 8-pin connector to address the electrical and packaging requirements. A typical module exhibited 3.5 dB noise figure, 23 dB of gain, .5 dB RMS amplitude error, and 7° RMS phase error from 7.0-10.0 GHz.

## INTRODUCTION

Communication systems realized with a phased array antenna offer several advantages over systems which utilize a conventional parabolic-dish antenna. These advantages include the ability to generate multiple independently steered antenna beams from a common aperture, the ability to make antennas conformal with their mounting structure, and the ability to produce directive beams that can rapidly be repositioned electronically.

This paper will describe the system requirements flowdown, the module and packaging design, and manufacture and test of a multi-chip MMIC module for the receive portion of a 7.0-10.0 GHz full-duplex dual-beam communication phased array antenna. This module features a single LTCC substrate to establish all DC, control, and RF interconnections, GaAs MMIC's for all RF functions, and silicon IC's for all control functions in a compact housing suitable for phased array integration requirements.

## MODULE OVERVIEW

The receive module block diagram is shown in Figure 1.

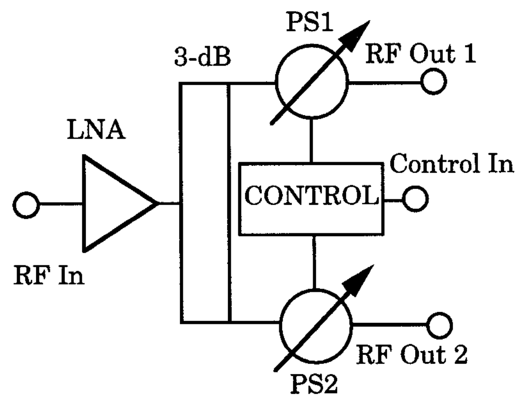


Figure 1 - Receive Module Block Diagram

The received signal(s) first enter a low-noise amplifier (LNA). This is used to set the module's noise figure and also contributes to the third-order-intercept (TOI) point for the two independent input signals. In order to minimize the development cost of this prototype system, limiter and circulator functions were not included in the module. The module will be protected through control of the operating environment. Two independently controlled 5-bit digital phase shifters follow the LNA and are fed from a 3-dB power divider. The phase shifters are used to electronically steer the two separate antenna beams.

RMS phase and amplitude errors over all phase states for an individual receive channel, as well as, RMS nominal gain errors from channel-to-channel and unit-to-unit must be minimized to ensure control of antenna



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side-lobe levels. The module phase errors over phase states and nominal insertion phase variations are accounted for by the phase shifters. For a system-level calibration, the phase shifters may also be used to account for phase errors in the antenna elements and beam-formers.

Since tapering of the receive signals was not required to meet the side-lobe requirements, a digital attenuator was not used. This minimized the module cost and complexity. An attenuator would be useful to ensure that all of the modules had the same nominal gain. The approach used to minimize this error was to exploit the array's 64 element size and to utilize LNA and phase shifter MMIC's from the same wafer lots.

A shift register and clock signal provide independent control signals for each bit of the digital phase shifters by converting an input serial data stream into parallel data lines. These signals are inverted to provide complements of the parallel signals necessary for the phase shifters. HEXFET's are used for control of the LNA bias.

## MODULE/PACKAGING DESIGN

Housing Design

The package size must be sufficiently small to prevent grating-lobe formation in the desired scan volume. To support a 10.5 GHz upper operating frequency limit with a 50° azimuth scan range and triangular lattice, the module width was set to 1.06". In the array, the module's receive input should be placed as close as possible to its corresponding antenna element in order to minimize loss (noise figure) between the module and element. Also, in a phased array all supporting electronics (beamformers, controllers, and power supplies) must be placed behind the antenna aperture to prevent blockage.

The controller, and DC power supplies are located behind the modules to minimize the spacing (loss) between the element and module. This dictates that the DC supply and controller interfaces be placed on the side of the module opposite of the antenna elements. The RF outputs are also on this side to provide a simple connection to the two RF beam-formers. This leads to an array design which utilizes modules placed side by side on horizontal slats in a classic "brick" topology shown in Figure 2.

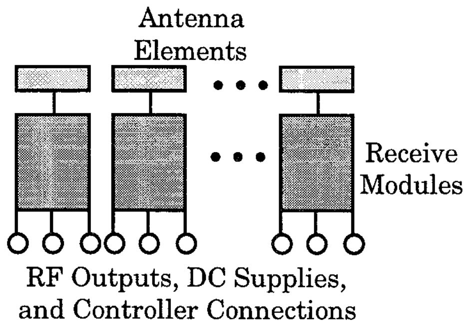


Figure 2 - Top View of a Slat for "Brick" Phased Array Architecture

To meet the challenging 1.06" width requirement, the phase shifters' ten command signals are fed to the module with a serial data stream to minimize the number of control lines into the module and, thereby, the DC/control connector size. Using this technique, the MMIC's and control IC's required a total of seven DC supply/control inputs into the module. A custom 8-pin DC connector with .018" diameter pins on .050" centers was used. The additional pin was included to provide flexibility for future increased functionality or re-design flexibility. Blind-mate connectors were used for all of the RF connections.

Another challenge in the design of the housing is the suppression of undesired cavity resonances. The cavity width is wide enough to support resonances within the desired band-width. The cavity width can be reduced electrically by utilizing a septum from the base of the housing which could be connected with a silver-loaded elastomer to the housing lid. A septum would increase the interconnection and assembly complexity, however, and preclude the use of a single substrate, which is necessary to minimize the assembly complexity.

Another technique to suppress the resonance is to load the cavity with ferrite material to lower the cavity Q. This method was implemented with some success with a .025" thick ferrite material attached to the housing lid. Measurements of the module with the LNA's replaced by 50Ω thin-film lines (only the LTCC Wilkinson divider and phase shifters) showed no resonances. When the LNA's were integrated, the input return loss did increase to approximately 6 dB at 10.5 GHz. If it is necessary for system performance, the input return loss could be improved by using a circulator between the antenna element and module.

## Substrate/Interconnect Design

The next challenge posed by the module width requirement is how the four RF components and four digital functions are connected with each other. The module width limitation and interconnect density precludes the use of a single-layer substrate technology. LTCC provides adequate RF performance at X-band and also provides a means for making interconnections in overlapping planes within the multi-layer structure.

A single LTCC substrate was used for all interconnections to simplify the module assembly and incorporated a 3-dB Wilkinson power divider. The LTCC was made with Dupont's 901 Au tape system, which features a 5.2 dielectric constant and .004" thick post-fired layers. The RF transmission lines were realized with 3 layer high microstrips with the RF ground plane buried within the LTCC. 7 additional layer were used to provide mechanical strength and DC supply and control interconnections. The microstrip ground plane was tied to the LTCC's bottom layer (housing) through quarter-wavelength spaced via's, which were placed in the vertical planes containing the outlines of the top layer microstrip. Additional via's were added at microstrip transition areas to suppress undesired modes.

The LNA minimizes system performance degradation due to loss in the LTCC Wilkinson combiner and subsequent microstrip lines. Therefore, for this application, LTCC insertion loss was not critical for system performance. The measured loss of the microstrips on three layers of 901 LTCC was estimated at .08 dB/mm, which may not be practical for all RF applications. The LTCC losses could have been minimized with the use of wider striplines or microstrips. These could have been realized by using a larger conductor to ground-plane spacing (more layers) to maintain the desired impedance levels.[1,2] The number of LTCC layers is directly proportional to the substrate cost, however, so only three LTCC layers were used to realize the microstrip lines. Fewer layers would have reduced the Wilkinson microstrip line widths below reasonable thick-film producibility guidelines.

Alumina thin-film substrates .010" thick were used to transition from the blind-mate RF pins to the LTCC microstrip lines. The use of thin-film substrates minimized packaging tolerance problems associated with the single piece LTCC substrate approach, allowed quick optimization of the RF transitions, and eliminated possible RF pin damage if rework involving LTCC substrate replacement was required. The thin-film substrates were mounted on .030" Molybdenum carriers to minimize the vertical distance to the LTCC and to permit a planar (lower cost) housing floor. Gold ribbon was used to make the connection between the RF pins and thin-film with a .010"x.001" gold ribbon. No additional compensation was necessary, and the RF pin-to-Alumina-to-LTCC transitions exhibited 18 dB return loss at 10.5 GHz.

## MMIC Design/Selection

Commercially available MMIC's were sought for this module, in order to minimize non-recurring engineering costs. A survey of the industry provided both PHEMT and MESFET based LNA's. MESFET LNA's generate a higher noise figure than PHEMT's but are generally less expensive. The desired communication data rate required the module to have 3.5 dB noise figure with a minimum of 20 dB of gain. In order to minimize cost while achieving the noise figure, the 64 units were populated with M/A Com's MESFET based MAAM71200, which typically provides 2.3 dB noise figure, +7 dBm ITOI, and 17 dB of gain from 7.5 to 12 GHz[3]. The third-order intercept point is important for experimental analysis of interference between two simultaneously received signals. Two of these MMIC's were used in series in each module to provide sufficient gain.

MESFET-based phase shifters were desired so that simple digital control signals could be used. 5-bits would allow the fifth bit to be used to compensate errors of the larger four bits to provide low error four-bit performance. The Westinghouse WPHS2580 digital

6-bit phase shifter meets these requirements and typically provides 4° RMS phase errors and .5 dB RMS amplitude errors[4]. This MMIC also provides +40 dBm ITOI so that it will not limit system TOI.

## MODULE MANUFACTURE/PERFORMANCE

### Module Manufacture

Each module contains 106 .001" wire-bonds to connect the MMIC's and digital IC's and requires approximately 6 hours of manual assembly and test time. Packaging materials, control IC's, and MMIC's cost $950/module. To date 48 modules have been started with 80% first-pass yield. A photograph of the receive module is shown in Figure 3.

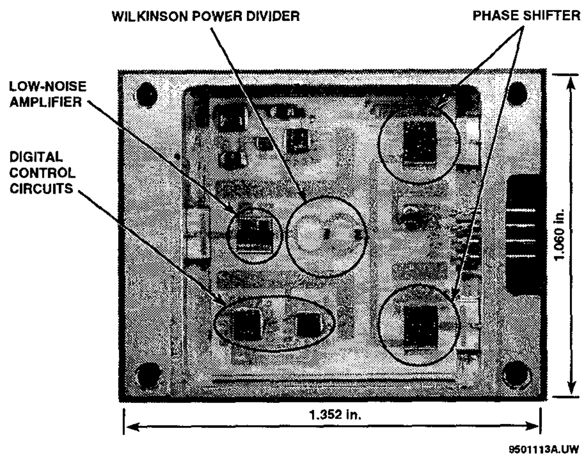


Figure 3 - Top View of Receive Module

### Module Performance

The RMS phase error performance of the 38 completed units is shown in Figures 4. Figure 5 shows the nominal and RMS gain error for these units. Typical module noise figure across the band-width is 3.5 dB.

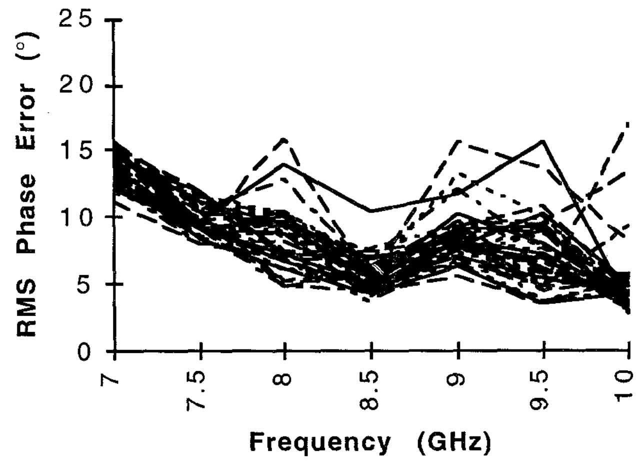


Figure 4 - RMS Phase Error for 38 Units

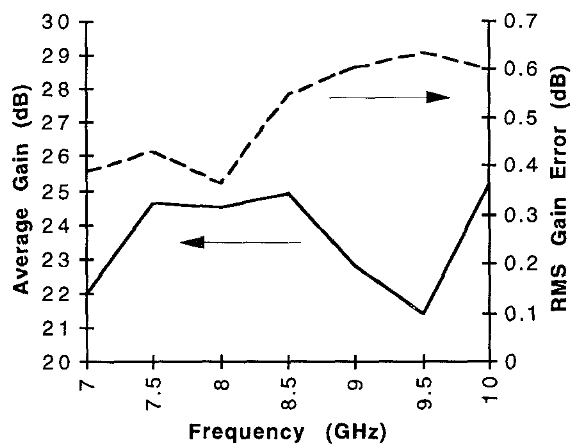


Figure 5 - Nominal Gain for 38 Units

## REFERENCES

[1] B. A. Kopp and A. S. Francomacaro, "Miniaturized Stripline Circuitry Utilizing LTCC," IEEE MTT-S, pp. 1513-1516, 1992.

[2] J. W. Gipprich, L. E. Dickens, J. A. Faulkner, "A Power Amplifier Yields 10 Watts over 8-14 GHz using GaAs MMIC's in an LTCC Serial Combiner/Divider Network," IEEE MTT-S, pp. 1369-1372, 1993.

[3] M/A Com MAAM 71200 Data Sheet

[4] Westinghouse WPHS2580 Data Sheet